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Peter Asbeck, Gabriel Rebeiz, James Buckwalter, Lawrence Larson, Sorin Voinigescu

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University of California - San Diego
Office of Contract & Grant Adm
9500 Gilman drive, MC 0934
La Jolla, CA 92093 -0934

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**14. ABSTRACT**
High efficiency, high power transmitters integrated in silicon at 45, 94 and 138 GHz were developed. Our approach employs CMOS-SOI and SiGe HBT unit amplifiers, power-combined in free-space using antenna arrays to attain high power levels. In the baseline approach, the signals are generated in separate modulator circuits, with external digital predistortion. In a companion approach, full signals are generated in free space, combining I and Q signals in the far field. In CMOS, stacked FET amplifiers have been used, and significant advances in the state-of-the-art were made. At 45GHz, a single CMOS chip produced an RF power of 630mW, which yielded an EIRP of

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| a. REPORT | b. ABSTRACT | c. THIS PAGE | | | Peter Asbeck |
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## Report Title

Final Report: High Efficiency mm-Wave Transmitter Array

## ABSTRACT

High efficiency, high power transmitters integrated in silicon at 45, 94 and 138 GHz were developed. Our approach employs CMOS-SOI and SiGe HBT unit amplifiers, power-combined in free-space using antenna arrays to attain high power levels. In the baseline approach, the signals are generated in separate modulator circuits, with external digital predistortion. In a companion approach, full signals are generated in free space, combining I and Q signals in the far field. In CMOS, stacked FET amplifiers have been used, and significant advances in the state-of-the-art were made. At 45GHz, a single CMOS chip produced an RF power of 630mW, which yielded an EIRP of 40 dBm using a contiguous 2x2 antenna array. At 94 GHz, a CMOS chip produced 250mW of RF power, yielding an EIRP of 33 dBm using a 2x4 antenna array on top of the Si IC. Output modulation was demonstrated up to 3 Gb/s (256QAM with 375MHz bandwidth, testbed limited). Combination of I and Q signals in the far field was demonstrated at 100GHz and 138GHz. RF output powers up to 13 dBm at 138GHz were measured with the corresponding I and Q channels. A separate on-chip power combined 125GHz amplifier demonstrated 22dBm output power.

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## Enter List of papers submitted or published that acknowledge ARO support from the start of the project to the date of this printing. List the papers, including journal references, in the following categories:

### (a) Papers published in peer-reviewed journals (N/A for none)

| Received | | Paper |
|---|---|---|
| 08/31/2013 | 11.00 | Bassel Hanafi, Fatih Golcuk, Amir Agah, James F. Buckwalter, Peter M. Asbeck, Hayg-Taniel Dabag. Analysis and Design of Stacked-FET Millimeter-Wave Power Amplifiers, IEEE Transactions on Microwave Theory and Techniques, (04 2013): 1543. doi: 10.1109/TMTT.2013.2247698 |
| 08/31/2013 | 12.00 | Andreea Balteanu, Ioannis Sarkas, Eric Dacquay, Alexander Tomkins, Gabriel M. Rebeiz, Peter M. Asbeck, Sorin P. Voinigescu. A 2-Bit, 24 dBm, Millimeter-Wave SOI CMOS Power-DAC Cell for Watt-Level High-Efficiency, Fully Digital m-ary QAM Transmitters, IEEE Journal of Solid-State Circuits, (05 2013): 1126. doi: 10.1109/JSSC.2013.2252752 |
| 10/14/2012 | 3.00 | Joohwa Kim, Hayg Dabag, Peter Asbeck, James F. Buckwalter. Q-Band and W-Band Power Amplifiers in 45-nm CMOS SOI, IEEE Transactions on Microwave Theory and Techniques, (06 2012): 0. doi: 10.1109/TMTT.2012.2193593 |
| 10/14/2012 | 4.00 | Arpit K. Gupta, Joohwa Kim, Peter Asbeck, James F. Buckwalter. A 9 mW, Q-Band Direct-Conversion I/Q Modulator in SiGe BiCMOS Process, IEEE Microwave and Wireless Components Letters, (06 2012): 0. doi: 10.1109/LMWC.2012.2197379 |
| 10/14/2012 | 5.00 | Arpit K. Gupta, James F. Buckwalter. Linearity Considerations for Low-EVM, Millimeter-Wave Direct-Conversion Modulators, IEEE Transactions on Microwave Theory and Techniques, (10 2012): 0. doi: 10.1109/TMTT.2012.2209435 |
| **TOTAL:** | | **5** |

**Number of Papers published in peer-reviewed journals:**

## (b) Papers published in non-peer-reviewed journals (N/A for none)

| Received | Paper |
|---|---|

**TOTAL:**

**Number of Papers published in non peer-reviewed journals:**

## (c) Presentations

**Number of Presentations:** 0.00

## Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

| Received | Paper |
|---|---|
| 09/01/2016 | 27.00 . A PMOS mm-wave power amplifier at 77 GHz with 90 mW output power and 24% efficiency, 2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC). 22-MAY-16, San Francisco, CA, USA. : , |
| 09/01/2016 | 30.00 . Series power combining: Enabling techniques for Si/SiGe millimeter-wave power amplifiers, 2016 IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF). 24-JAN-16, Austin, TX, USA. : , |
| 09/01/2016 | 32.00 . 28 GHz >250 mW CMOS Power Amplifier Using Multigate-Cell Design, 2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS). 11-OCT-15, New Orleans, LA, USA. : , |
| 09/01/2016 | 38.00 . A 11% PAE, 15.8-dBm two-stage 90-GHz stacked-FET power amplifier in 45-nm SOI CMOS, 2013 IEEE/MTT-S International Microwave Symposium - MTT 2013. 02-JUN-13, Seattle, WA, USA. : , |

**TOTAL:** **4**

**Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts):**

## Peer-Reviewed Conference Proceeding publications (other than abstracts):

| Received | Paper |
|---|---|
| 08/22/2011 | 2.00 Sataporn Pornpromlikit, Hayg-Taniel Dabag, Bassel Hanafi, Joohwa Kim, Lawrence E. Larson, James F. Buckwalter, Peter M. Asbeck. A Q-Band Amplifier Implemented with Stacked 45-nm CMOS FETs, Compound Semiconductor IC Symp.. 16-OCT-11, . : , |
| 08/30/2015 | 19.00 Youjiang Liu, Gang Liu, Peter M. Asbeck. Frequency quadrupling transmitter architecture with digital predistortion for high-order modulation signal transmission, 2015 IEEE Radio and Wireless Symposium (RWS). 24-JAN-15, San Diego, CA, USA. : , |
| 08/30/2015 | 20.00 Po-Yi Wu, Youjiang Liu, Bassel Hanafi, Hayg Dabag, Peter Asbeck, James Buckwalter. A 45-GHz Si/SiGe 256-QAM transmitter with digital predistortion, 2015 IEEE MTT-S International Microwave Symposium (IMS2015). 16-MAY-15, Phoenix, AZ, USA. : , |
| 08/31/2013 | 13.00 Amir Agah, Wei Wang, Peter Asbeck, Lawrence Larson, James Buckwalter. A 42 to 47-GHz, 8-bit I/Q digital-to-RF converter with 21-dBm P<inf>sat</inf> and 16% PAE in 45-nm SOI CMOS, 2013 IEEE Radio Frequency Integrated Circuits Symposium (RFIC). 01-JUN-13, Seattle, WA, USA. : , |
| 09/01/2016 | 1.00 Hayg-Taniel Dabag, Joohwa Kim, Lawrence E. Larson, James F. Buckwalter, Peter M. Asbeck. A 45 GHz SiGe HBT Amplifier with Greater Than 25% Efficiency and 30mW Saturated Output Power, Bipolar Circuits and Technology Meeting. 09-OCT-11, Minneapolis USA. : , |
| 09/01/2016 | 26.00 S. P. Voinigescu, S. Shopov, A. Balteanu, I. Sarkas. Mm-wave power-DAC transmitters with transistor and antenna segmentation, 2014 IEEE International Microwave and RF Conference (IMaRC). 15-DEC-14, Bangalore, India. : , |
| 09/01/2016 | 21.00 Sorin P. Voinigescu, Stefan Shopov. An 8-Bit 140-GHz Power-DAC Cell for IQ Transmitter Arrays with Antenna Segmentation, 2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS). 18-OCT-14, La Jolla, CA, USA. : , |
| 09/17/2013 | 15.00 Jefy Jayamon, Amir Agah, Bassel Hanafi, Hayg Dabag, James Buckwalter, Peter Asbeck. A W-band stacked FET power amplifier with 17 dBm P<inf>sat</inf> in 45-nm SOI CMOS, 2013 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in Rf Systems (SiRF). 20-JAN-13, . : , |
| 10/14/2012 | 6.00 Ioannis Sarkas, Andreea Balteanu, Eric Dacquay, Alexander Tomkins, Sorin Voinigescu. A 45nm SOI CMOS Class-D mm-Wave PA with10Vpp differential swing, 2012 IEEE International Solid- State Circuits Conference - (ISSCC). 18-FEB-12, San Francisco, CA, USA. : , |
| 10/14/2012 | 7.00 Andreea Balteanu, Ioannis Sarkas, Eric Dacquay, Alex Tomkins, Sorin P. Voinigescu. A 45-GHz, 2-bit power DAC with 24.3 dBm output power, 14 Vpp differential swing, and 22% peak PAE in 45-nm SOI CMOS, 2012 IEEE Radio Frequency Integrated Circuits Symposium (RFIC). 16-JUN-12, Montreal, QC, Canada. : , |
| 10/14/2012 | 8.00 Hayg-Taniel Dabag, Peter M. Asbeck, James F. Buckwalter. Linear operation of high-power millimeter-wave stacked-FET PAs in CMOS SOI, 2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS). 04-AUG-12, Boise, ID, USA. : , |

| | | |
|---|---|---|
| 10/14/2012 | 9.00 | Amir Agah, Bassel Hanafi, Hayg Dabag, Peter Asbeck, Lawrence Larson, James Buckwalter. A 45GHz Doherty power amplifier with 23% PAE and 18dBm output power, in 45nm SOI CMOS, 2012 IEEE/MTT-S International Microwave Symposium - MTT 2012. 16-JUN-12, Montreal, QC, Canada. : , |
| 10/14/2012 | 10.00 | James Buckwalter, Amir Agah, Hayg Dabag, Bassel Hanafi, Peter Asbeck, Lawrence Larson. A 34% PAE, 18.6dBm 42-45GHz stacked power amplifier in 45nm SOI CMOS, 2012 IEEE Radio Frequency Integrated Circuits Symposium (RFIC). 16-JUN-12, Montreal, QC, Canada. : , |
| **TOTAL:** | **13** | |

**Number of Peer-Reviewed Conference Proceeding publications (other than abstracts):**

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## (d) Manuscripts

| | |
|---|---|
| Received | Paper |

**TOTAL:**

**Number of Manuscripts:**

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## Books

| | |
|---|---|
| Received | Book |

**TOTAL:**

| Received | Book Chapter |
|---|---|

09/01/2016 34.00 . Stacked-transistor mm-wave power amplifiers, : Cambridge University Press, ( 2016)

**TOTAL:** **1**

## Patents Submitted

## Patents Awarded

## Awards

Gabriel Rebeiz was elected to the National Academy of Engineering, 2016
Gabriel Rebeiz received the IEEE Daniel Noble Award, 2014
Peter Asbeck received the IEEE Microwave Theory and Techniques Society Distinguished Educator Award, 2012

## Graduate Students

| NAME | PERCENT_SUPPORTED | Discipline |
|---|---|---|
| Hayg Dabag | 0.80 | |
| Bassel Hanafi | 1.00 | |
| Jefy Jayamon | 1.00 | |
| Narek Rostomyan | 0.80 | |
| Fatih Golcuk | 0.40 | |
| Arpit Gupta | 1.00 | |
| Amir Agah | 1.00 | |
| Po-Yi Wu | 1.00 | |
| Joohwa Kim | 0.40 | |
| Chih-Hsiang Ko | 0.30 | |
| Ozan Gurbuz | 1.00 | |
| Ken Lin | 0.50 | |
| Tao Yang | 0.30 | |
| Ioannis Sarkas | 0.80 | |
| Andreea Balteanu | 0.80 | |
| Stefan Shopov | 0.90 | |
| Michael Kalajian | 0.20 | |
| Alexander Tomkins | 0.20 | |
| **FTE Equivalent:** | **12.40** | |
| **Total Number:** | **18** | |

## Names of Post Doctorates

| NAME | PERCENT_SUPPORTED |
|---|---|
| Young-Pyo Hong | 0.20 |
| Youjinag Liu | 0.10 |
| Gang Liu | 0.20 |
| Saeed Daneshgar | 0.40 |
| **FTE Equivalent:** | **0.90** |
| **Total Number:** | **4** |

## Names of Faculty Supported

| NAME | PERCENT_SUPPORTED | National Academy Member |
|---|---|---|
| Peter Asbeck | 0.10 | Yes |
| Gabriel Rebeiz | 0.10 | Yes |
| Sorin Voinigescu | 0.10 | |
| James Buckwalter | 0.10 | |
| Lawrence Larson | 0.05 | |
| **FTE Equivalent:** | **0.45** | |
| **Total Number:** | **5** | |

## Names of Under Graduate students supported

| NAME | PERCENT_SUPPORTED |
|---|---|
| **FTE Equivalent:** | |
| **Total Number:** | |

## Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

The number of undergraduates funded by this agreement who graduated during this period: ..... 0.00

The number of undergraduates funded by this agreement who graduated during this period with a degree in science, mathematics, engineering, or technology fields:..... 0.00

The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields:..... 0.00

Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale):..... 0.00

Number of graduating undergraduates funded by a DoD funded Center of Excellence grant for Education, Research and Engineering:..... 0.00

The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense ..... 0.00

The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields:..... 0.00

## Names of Personnel receiving masters degrees

| NAME |
|---|
| **Total Number:** |

## Names of personnel receiving PHDs

| NAME | |
|---|---|
| Bassel Hanafi | |
| Hayg Dabag | |
| Fatih Golcuk | |
| Arpit Gupta | |
| Amir Agah | |
| Po-Yi Wu | |
| Joohwa Kim | |
| Chih-Hsiang Ko | |
| Ozan Gurbuz | |
| Ken Lin | |
| Ioannis Sarkas | |
| Andreea Balteanu | |
| **Total Number:** | **12** |

## Names of other research staff

| NAME | PERCENT_SUPPORTED |
|---|---|
| **FTE Equivalent:** | |
| **Total Number:** | |

## Sub Contractors (DD882)

## Inventions (DD882)

## Scientific Progress

See attachment

## Technology Transfer

## Scientific Progress and Accomplishments

The objective of this program has been to develop high efficiency, high power transmitters integrated in silicon at 45 GHz, 94 GHz and 138 GHz. Our approach has been based on the development of high power unit amplifier cells using advanced Si technologies (CMOS-SOI and SiGe HBT), whose output is power-combined in free-space using antenna arrays to attain high power levels. The signals to be transmitted are generated and linearized in separate modulator circuits, together with digital predistortion carried out externally within the baseline program. In a parallel approach, signal generation is carried out in the same integrated circuits as the power amplifiers (representing a "power-DAC" implementation), and the power combination of I, Q signals in the far field is utilized to form the desired signal constellations.

Numerous scientific and technology advancements were made in the program. To increase output power and efficiency using Si CMOS technology, stacking of transistors was extensively analyzed and demonstrated experimentally at frequencies ranging from 15GHz to 140GHz. Antenna arrays driven by single chip CMOS power amplifiers attained record power and efficiency at 45 GHz (630mW) and 94 GHz (250 mW). On-chip power combining using various transmission line and balun approaches was also demonstrated; SiGe HBT amplifiers were designed and measured with state-of-the-art output power at 80 GHz (27 dBm) and 120GHz (21 dBm). Signal generation with complex constellations formed in the far field was shown for the first time. Modulation of radiated outputs at high rates and with complex constellations (up to 256 QAM for 45 GHz arrays) was demonstrated. Doherty amplifiers were demonstrated in Si technology at mm-wave frequencies for the first time. It was shown that with scaled CMOS pMOS – based power amplifiers had a variety of advantages over nMOS PAs. Advancements have been reported in detail in numerous publications (13 journal papers, 15 conference papers), and are briefly summarized in the following.

### CMOS Stacking for Power Amplifiers

The stacking of multiple FETs allows increasing drain supply voltage, which in turn allows higher output power and a broader bandwidth output matching network. Our research studied stacked-FET CMOS mm-wave with a focus on design of appropriate complex impedances between the transistors. Figure 1 illustrates a 4 stack amplifier, with shunt inductances for reactive impedance matching at the lowest stacking node and series inductance in the 2nd stacked node. Different matching techniques for the intermediate nodes were used in 2-, 3- and 4-stack single-stage Q-band CMOS power amplifiers (PAs). The 4-stack design achieves a saturated output power above 21 dBm while achieving a maximum power-added-efficiency (PAE) above 20

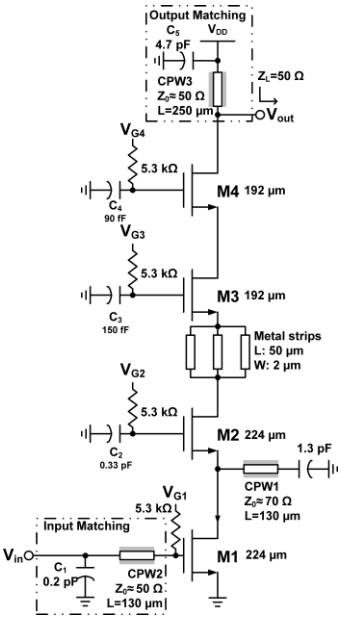

Fig.1: Stacked nMOS FET 45 GHz power amplifier.

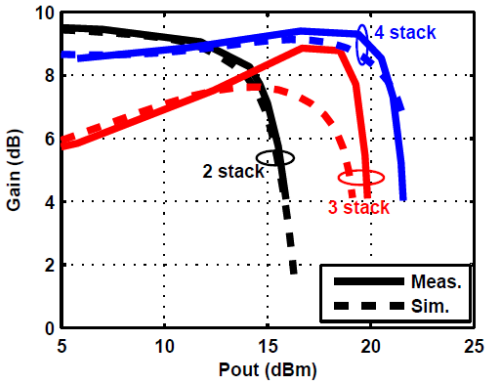


Fig.2: Measured and simulated gain vs output power for various stacked FET Pas.

% from 38 GHz to 47 GHz. The effectiveness of an inductive tuning technique is demonstrated in measurement, improving the PAE from 26 % to 32 % in a 2-stack design. The input and output matching network are designed using on-chip shielded coplanar waveguide (CPW) transmission lines as well as metal finger capacitors. The amplifiers were implemented in a 45-nm CMOS silicon-on-insulator (SOI) process. Each of the amplifiers occupies an area of 600 um x 500 um including pads. Simulated amplifier performance is in good accord with the measurements, as shown in figure 2. The increase in output power obtained via stacking is illustrated in figure 3. Stacking was demonstrated up to 94 GHz in simple FET structures, for which output power reached.

Using Si CMOS on insulator technology (at the 45nm node), compact, high power amplifiers were attained using stacked MOSFETs, as previously reported. In the most recent technique, the MOSFETs were arranged in a multigate fashion, as shown in Fig. 4. In order to maintain adequate voltage handling, capacitors are attached to the gates of the individual units. These capacitors are incorporated directly within the unit cell by using the multiple metal layers available within the CMOS technology. The resultant structure can be replicated in arrays to form high power cells. The technique was tested at relatively low frequency (28GHz) because in the initial embodiment, matching at higher frequencies was not optimal. The matched

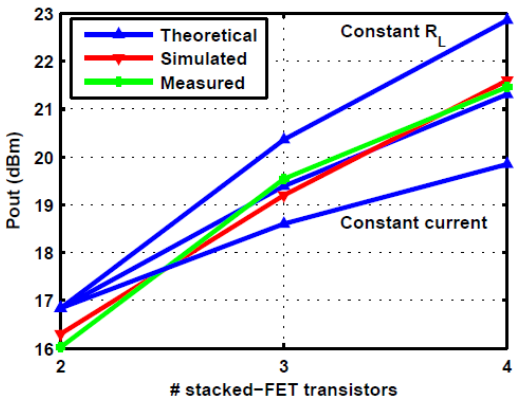


Fig.3: Variation of output power with number of stacked FETs, for constant current and constant RL scaling and for measured circuits.

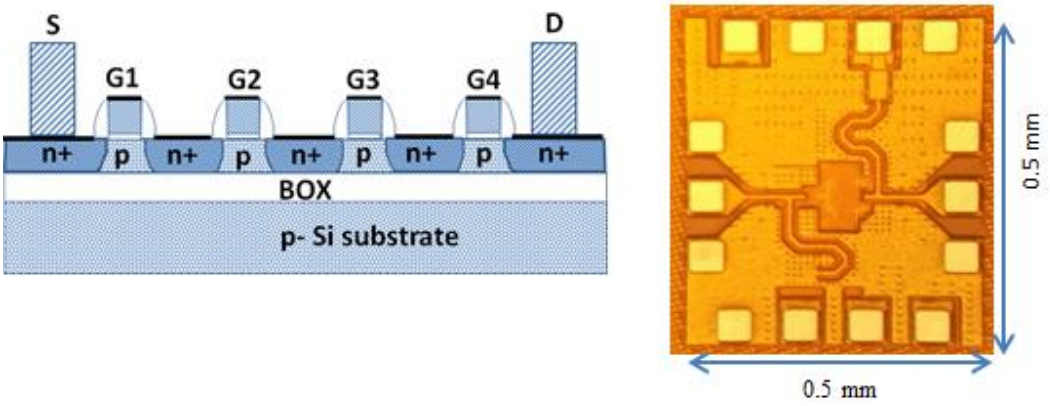


Fig. 4: Multigate structure of stacked FET unit cell, and chip photo of completed 28GHz stacked FET power amplifier.

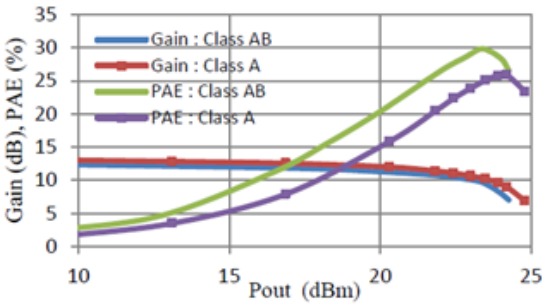


Fig. 5: Gain and PAE vs output power for multigate stacked FET PA.

amplifier has very small size (active element 150um x 80um). Measurement results are shown in Fig. 5, illustrating output power up to 300mW (Class A bias), and efficiency up to 29% (Class AB bias).

**Power Combining with Antenna Arrays**

Antennas were designed and fabricated to enable spatial power-combining of the outputs of unit power amplifiers. Assemblies were then produced incorporating both power amplifier ICs and antennas. Figure 6 shows the schematic diagram and implemented system for a 2x2 antenna/amplifier array at 45 GHz. The radiated output beam profile agrees with calculations, as shown in fig. 7. The peak EIRP for the single chip reached 10W for the chip; using a calculated antenna gain of 12dB, the power supplied by the chip at 45GHz was 630mW. On a separate board, a 2x8 array of antennas was implemented, fed by 4 CMOS chips. For this structure, the peak EIRP was 100W, and the aggregate RF output power at 45 GHz was 2.0W.

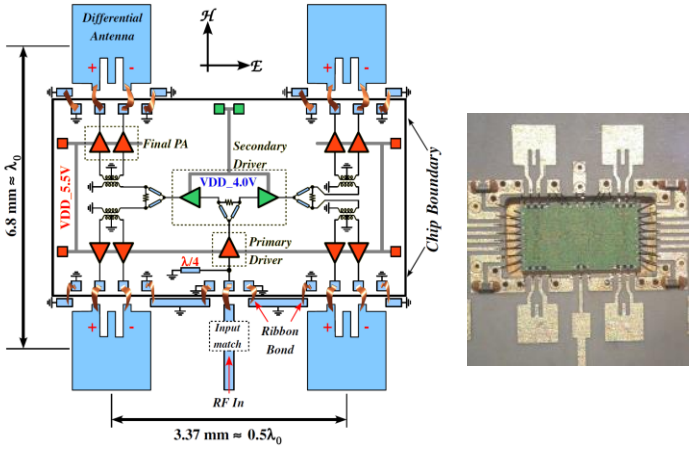


Fig.6: Schematic diagram and implemented structure of 45 GHz 2x2 CMOS amplifier /antenna array.

Experiments were undertaken to modulate the high power amplifier arrays, initially using external modulators and a custom high bandwidth digital predistortion system. The experiments showed that the array output could be linearized very effectively over a broad bandwidth, with sufficiently small error-vector magnitude that complex constellations could be transmitted. In fig. 8 is shown the signal constellations of the received and demodulated waveforms, for filtered 1024 QAM modulation having a

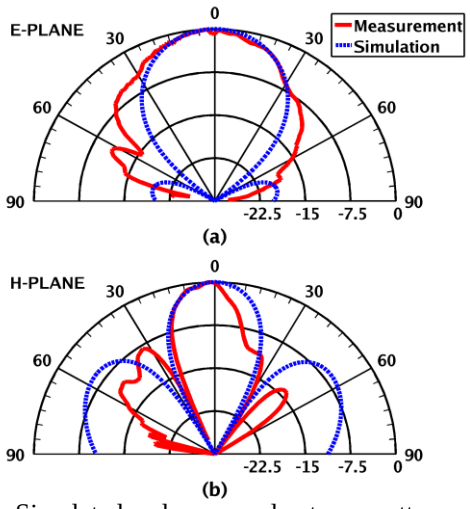


Fig.7: Simulated and measured antenna patterns for 45 GHz 2x2 array.

signal bandwidth of 100MHz, before and after digital predistortion (DPD). With DPD the EVM is found to decrease from 6.4% to 1.3%. With predistortion, a low error rate (below 0.001) was obtained. The figure shows explicitly where errors are located, demonstrating that the noise is not customary Additive White Gaussian Noise. The overall transmitted data rate is approximately 1 Gb/sec (10 bits per symbol with 100Msymbols per second). This is promising for future communication systems with high spectral efficiency.

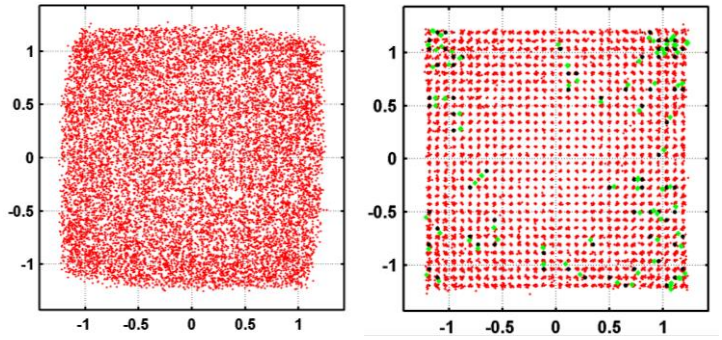


Fig.8: Received signal constellations for 1024 QAM signal transmitted by 2x2 array, before and after digital predistortion. For the DPD case, green points mark the bit errors.

Assemblies of power amplifiers and antennas were also implemented for operation at 94 GHz. In fig. 9 is shown the schematic structure and implemented system consisting of a single CMOS chip containing 8 differential power amplifiers, and a 2x4 array of antennas located on a quartz superstrate. The overall system was measured to have the antenna pattern shown in Fig. 10, in good agreement with simulations. The peak EIRP for the radiated power was 2W. Using the simulated antenna gain of 9 dB, the calculated RF power provided by the CMOS chip was 250mW. Both the results at 45 GHz and at 94 GHz are records for CMOS power amplifier output power.

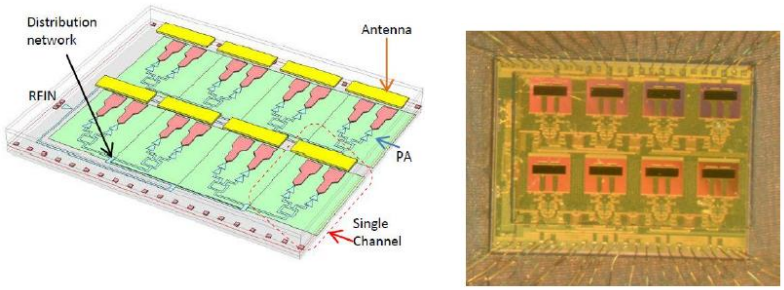


Fig.9: Schematic diagram and implemented structure for 94 GHz power amplifier / antenna array.

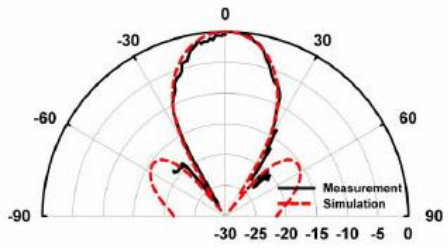


Fig. 10: Simulated and measured antenna pattern for 94 GHz 2x4 amplifier / antenna array.

Using an external modulator, upconverter and downconverter, measurements were made of modulated signals radiated from the 94 GHz amplifier / antenna array reported last year. The overall measurement system is shown in Fig. 11. Using digital predistortion, excellent signal constellations could be obtained for complex modulations. In Fig. 6 is shown the detected result for 256 QAM signals, with a symbol rate of 375 GS/s (for a total modulation rate of 3 Gb/s. The corresponding EVM was 2.5 %

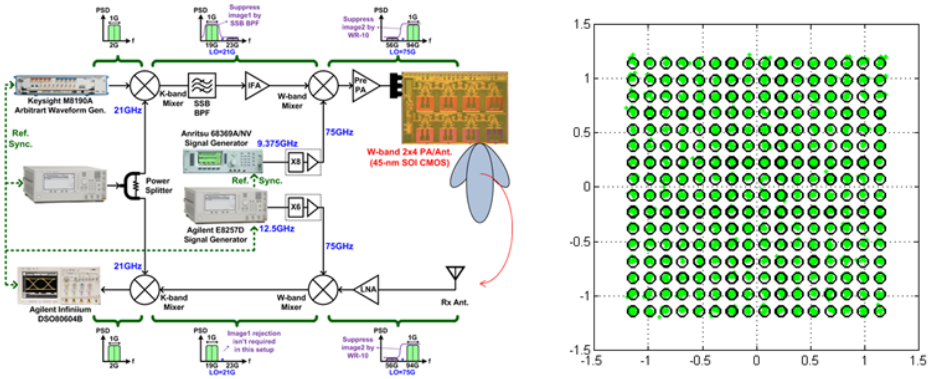


Fig. 11: Modulation, measurement and DPD system, and captured signal constellation for 94 GHz amplifier / antenna array, transmitting 3 Gb/s 256 QAM signals.

## On-Chip Combining of Power Amplifiers

At a frequency of 80 GHz, a series of SiGe HBT-based power amplifiers were designed which employed on-chip corporate power combining in order to achieve high output power. The largest amplifier, shown in Fig. 12, achieved a record output power of 560mW, a milestone for Si-based technology to exceed 0.5W at such a high frequency. Unit amplifiers are based on common-emitter stages; 3stages are incorporated in order to achieve high gain (18dB); PAE reached a maximum of 10%.

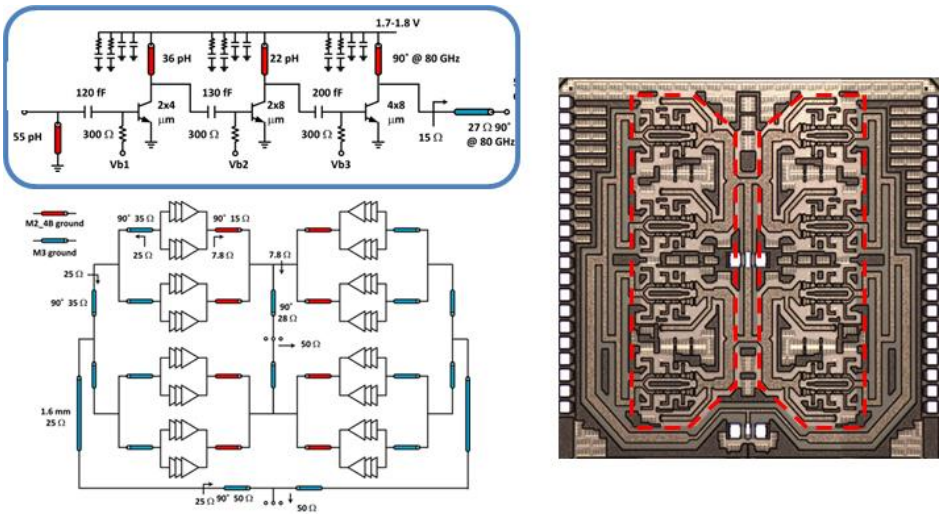


Fig. 12: 3 stage unit cell, block diagram and chip photo of 16-way power combined SiGe power amplifier with record 560mW output.

Power amplifier circuits were demonstrated using SiGe HBT/BiCMOS technology with on-chip baluns designed in a compact fashion by incorporating device capacitances within the transmission lines. The unit amplifiers are based on cascode cells. Record output power at 125 GHz was obtained, up to 22dBm. The corresponding circuit diagram and output power are shown in Fig.13.

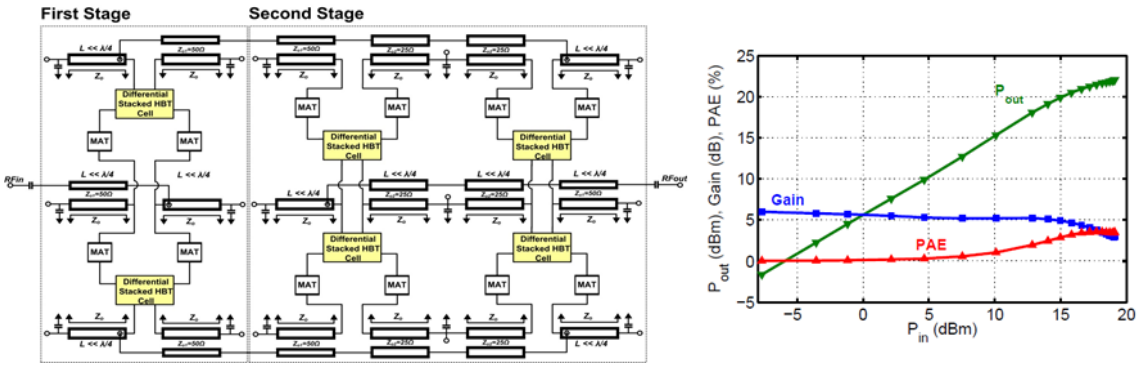


Fig.13: Circuit diagram and output power, gain and PAE of 125GHz amplifier implemented with SiGe HBT technology, using compact transmission line baluns.

CMOS FET stacking was also employed in order to increase the output power attained with frequency multipliers. Using the arrangement shown in Fig. 14, a push-push frequency doubler was demonstrated in which output power reached 5 dBm at 200 GHz.

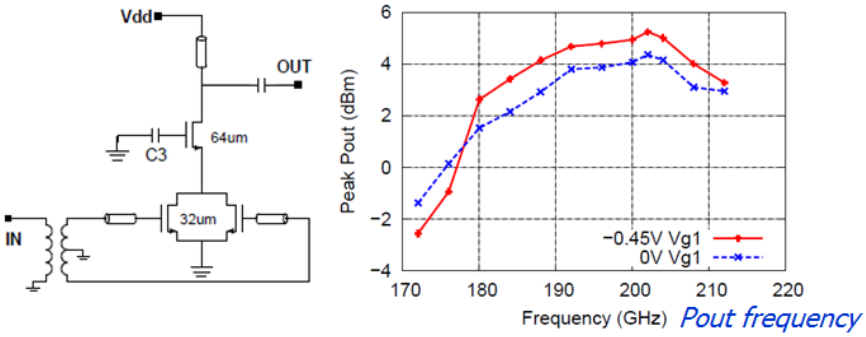


Fig. 14: Circuit diagram and measured output power of stacked FET frequency doubler implemented with 45nm CMOS SOI

## Signal Generation and Modulator Circuits

A modulator/upconverter circuit developed in this program is shown in figure 15 (which includes both block diagram and layout). I-Q DACs with 12 bit resolution were incorporated, followed by a quadrature modulator optimized for operation at 45 GHz. EVM below 2.5% was obtained for 64QAM signals, which is a record for Q-band systems.

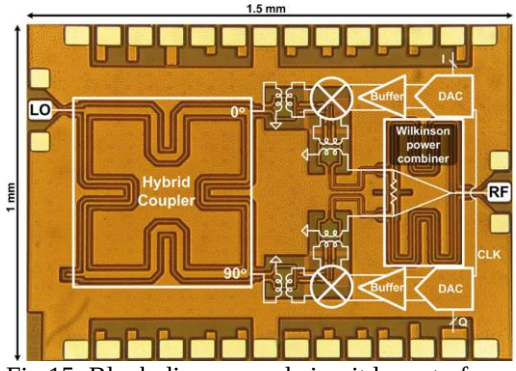


Fig.15: Block diagram and circuit layout of 45GHz direct I/Q modulator.

Direct digital modulator / upconverter / power amplifier combinations were demonstrated using stacked FET techniques, in which outputs could be modulated at low resolution (1 or 2 bits), in a configuration such that with free-space combining of the outputs of multiple unit circuits, complex constellations with high resolution and low EVM could be obtained. Figure 16 illustrates the simple signal constellations obtained with a building block modulator, and the constellation that emerges with an array of the modulator/ amplifiers. A proof-of-concept 2-bit polar modulated power DAC cell was fabricated in 45-nm SOI CMOS and operates at 45 GHz with a saturated output power (PSAT) larger the 24 dBm. The measured Binary Phase Shift Keying (BPSK) and Amplitude Shift Keying (ASK) modulation data rates exceed 2.5 Gb/s and 1.25 Gb/s, respectively, for carriers in the 45 to 50 GHz range. The circuit is implemented with stacked FETs in differential fashion, pictured in Fig. 17. Inductors between FETs improve the overall frequency response by compensating capacitance at the intermediate nodes.

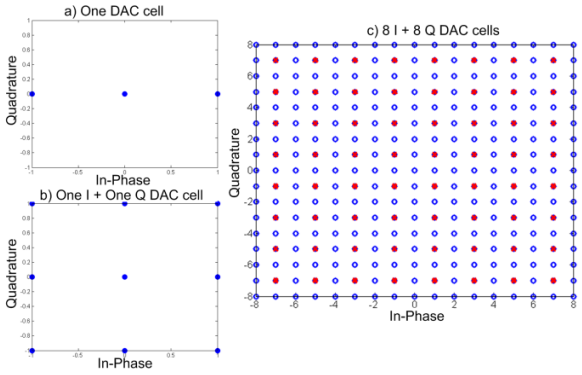


Fig.16: Signal constellations for building block modulator / amplifiers, and simulated constellation for free-spaced combined array of 8 DAC pairs.

Demonstrations have been done of exceptionally broadband modulation capability in CMOS chips, at carrier frequencies up to 100 GHz. Figure 17 illustrates a CMOS chip containing multiple "power DACs" driven by a mm-wave carrier LO input, along with modulation data. It was demonstrated that the chip could provide modulated output with input data at rates as high as

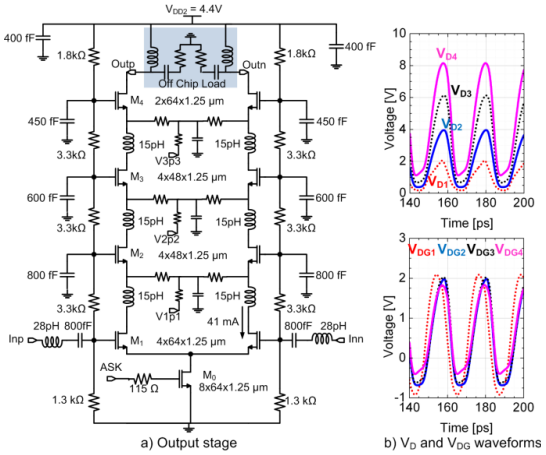


Fig.17: Circuit diagram and simulated waveforms for stacked FET modulator / power amplifier.

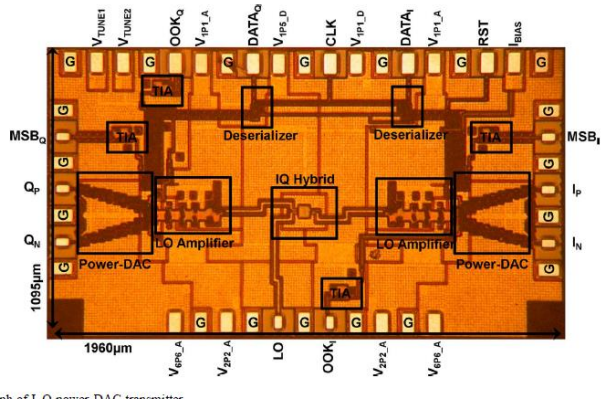


Fig. 17: Fabricated CMOS power DAC providing 4 modulated outputs.

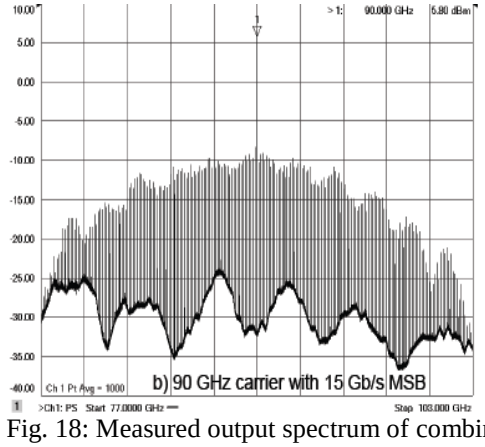


Fig. 18: Measured output spectrum of combined modulator/power amplifier with 90GHz carrier and 15 Gb/s On-Off keying modulation.

15 Gb/s, as shown in Fig. 18. In the experiment, a single bit is modulated with a pseudorandom sequence (since sources are currently unavailable to provide more than that at the highest speeds). The output spectrum is found to agree with expectations.
Signal generation in the far-field was also demonstrated with this technique, at frequencies in the range 100-140GHz. For this, a chip was configured with two channels, one for I and one for Q signals, each configured to allow amplitude 0 or 1 (1 amplitude bit) and phase 1 or -1 (one phase bit). The input bits could be modulated at very high rates. The chip coupled directly to patche antennas (one for each channel) mounted on top of the chip on a quartz superstrate (Fig. 19). Far field patterns showed successful generation of complex patterns, such as shown in Fig. 20. The high data rtes achieved are also evident in Fig.20, which shows measured EVM for different modulation formats. QPSK is found to yield the highest performance links.

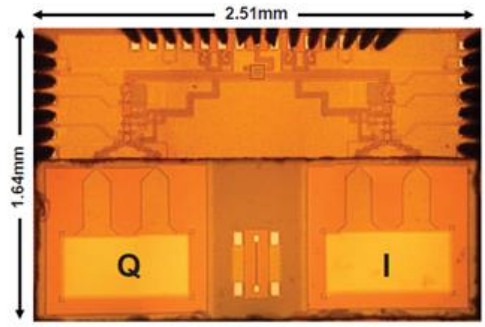


Fig. 19: Chip photo of 2 channel 100GHz power-DAC with I and Q patch antennas on quartz superstrate.

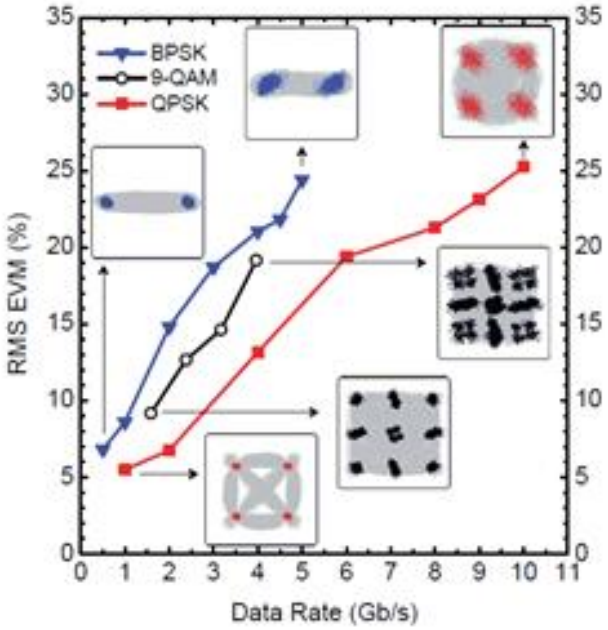


Fig. 20: Measured eye diagrams and error vector magnitude obtained at various bit rates for multiple modulation formats.